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Description

[High-Voltage Input Tolerant Receiver]

BACKGROUND OF INVENTION

[0001] Field of the Invention

[0002] This invention relates to a high-voltage input tolerant receiver, and more particularly, to a high-voltage input tolerant receiver, which receives an external signal varying between ground and a high voltage limit of the internal elements of the receiver, and outputs an internal signal varying between ground and just below the high voltage limit of the internal elements of the receiver.

[0003] Background of the Invention

[0004] There is a high-voltage input tolerant receiver as shown in Fig. 3 used as an interface from a 5V driving element to 3.3V driving element. Referring to Fig. 3, a conventional high-voltage input tolerant receiver 100 includes a PAD 2, a clamp circuit 31, a level keeper 60, a buffer circuit 15, and a hysteresis circuit 5. The clamp circuit 31, connected between the output node of the PAD 2 and the input node

of an inverter IV1 in the buffer circuit 15, has an n-channel MOS transistor N1 with its gate connected to a 3.3V power-supply potential node 10. The level keeper 60 has a p-channel MOS transistor P9. The p-channel MOS transistor P9, connected between the 3.3V power-supply potential node 10 and the input node of the inverter IV1, receives at its gate an output signal from the inverter IV1. In the buffer circuit 15, inverters IV1 to IV4 are connected in series so that an internal signal ϕB will be output from the inverter IV4.

[0005] When an external signal ϕC input from PAD 2 is less than $3.3V-V_{thN1}$, the clamp circuit 31 outputs an intermediate signal ϕD equivalent to the external signal ϕC, where V_{thN1} is a threshold voltage of the n-channel MOS transistor N1. Conversely, when the external signal ϕC exceeds $3.3V-V_{thN1}$, the clamp circuit 31 clamps the intermediate signal ϕD to $3.3\ V-V_{thN1}$, which prevents the internal elements of the high-voltage input tolerant receiver 100 from being damaged or destroyed by high voltage signals.

[0006] When the intermediate signal ϕD is clamped to $3.3V-V_{thN1}$, the p-channel MOS transistor P9 in the level keeper 60 is turned on, pulling the intermediate signal ϕD input to the inverter IV1 up to 3.3V, which prevents shoot-

through current from flowing into the inverter IV1.

[0007] Fig. 4 shows variations of the intermediate signal ϕD and internal signal ϕB, and variations of current I1 flowing from the level keeper 60 as the external signal ϕC varies from 0V to 5.5V.

[0008] Referring to Fig. 4, the external signal ϕC varies from 0V to 3.3V during the period from time t10 to time t20. During this period, the intermediate signal ϕD output from the clamp circuit 31 is equivalent to the external signal ϕC. After time t20, the external signal ϕC exceeds $3.3V-V_{thN1}$, and the clamp circuit 31 clamps the intermediate signal ϕD to $3.3V-V_{thN1}$. Since the potential difference between the clamped intermediate signal ϕD and the ground potential GND exceeds a threshold voltage V_{thN2} of an n-channel MOS transistor N2, current flows into the n-channel MOS transistor N2 in the inverter IV1 to turn on the n-channel MOS transistor N2, allowing the inverter IV1 to output a 0V signal. At this time, since the potential difference between the 0V output signal from the inverter IV1 and the 3.3V power-supply potential exceeds a threshold voltage V_{thP9} of the p-channel MOS transistor P9, the p-channel MOS transistor P9 is turned on. As a result, the level keeper 60 pulls up the intermediate signal

ϕD, and at time t30, the intermediate signal ϕD becomes 3.3V. After the intermediate signal ϕD is pulled up to 3.3V, only the n-channel MOS transistor N2 in the inverter IV1 is in operation, thereby preventing the shoot-through current.

[0009] Then, after time t40, the level of the external signal ϕC is reduced, and at time t50, although it becomes lower than that of the intermediate signal ϕD, since the level keeper 60 is active, the intermediate signal ϕD is maintained at 3.3V. Ultimately, at time t60, at which point the level keeper 60 goes beyond being tolerant of the voltage drop of the external signal ϕC, the p-channel MOS transistor P9 is turned off, and the voltage level of the intermediate signal ϕD becomes equal to that of the external signal ϕC just after time t60.

[0010] The high-voltage input tolerant receiver 100 uses the clamp circuit 31 to protect the 3.3V driving elements and the level keeper 60 to prevent the occurrence of shoot-through current in the inverter IV1. Such a high-voltage input tolerant receiver 100, however, causes the following problems.

[0011] (1) Analog signals are distorted in the high-voltage input tolerant receiver.

[0012] In the high-voltage input tolerant receiver 100, when the external signal ϕC is higher than $3.3V-V_{thN1}$, the intermediate signal ϕD is clamped to $3.3V-V_{thN1}$. In this case, the intermediate signal ϕD does not accord with the external signal ϕC, creating distortion. When the external signal ϕC is a digital signal distortion is not a concern, but for analog signals the distortion can be significant.

[0013] (2) The reset function does not work in a reset circuit using the high-voltage input tolerant receiver.

[0014] In a reset circuit 200 shown in Fig. 5, when a driver 300 has low drive power, even if a logic Low level signal is output from the driver 300, it will not become a perfect 0V signal. Since the high-voltage input tolerant receiver 100 has the hysteresis circuit 5, the high-voltage input tolerant receiver 100 will evaluate whether any input signal is at a logic high level unless the input signal into the high-voltage input tolerant receiver 100, that is, the external signal ϕC, becomes equal to or lower than a logic low level threshold voltage Vil interpreted by the hysteresis circuit 5. As a result, the level keeper 60 continues to operate so that the high-voltage input tolerant receiver 100 will continuously output the logic high signal without being reset. This problem arises when sink current flow-

ing into the driver 300 is smaller than the sum of current I2 flowing into a pull-up resistor R100 and current I1 flowing from the level keeper 60 in the high-voltage input tolerant receiver 100.

[0015] (3) Unnecessary current I1 flows from the level keeper 60.

[0016] Current I1 flows from the level keeper 60 to the outside during the period from time t20 to time t30 and after time t60 in Fig. 4 and causes unnecessary power consumption.

[0017] Japanese Patent Laid-Open No. 2000-278113 discloses an example of an input/output circuit with the above described deficiencies with respect to distortion of analog signals and power dissipation.

Summary of Invention

[0018] It is an object of the invention to provide a high-voltage input tolerant receiver capable of reducing the distortion of analog signals.

[0019] It is another object of the invention to provide a high-voltage input tolerant receiver capable of achieving power savings.

[0020] According to the invention, a high-voltage input tolerant receiver is disclosed that receives an external signal varying between ground and a high voltage limit of the inter-

nal elements of the receiver and outputs an internal signal varying between ground and just below the high voltage limit of the internal elements of the receiver. The high-voltage input tolerant receiver includes a pad, a control circuit, a first clamp circuit, a level keeper circuit, and a buffer circuit. The pad receives the external signal. The control circuit receives the external signal input from the pad, and outputs a first control signal and a second control signal when the external signal is higher than a first voltage. The first clamp circuit receives the external signal input from the pad, outputs an intermediate signal equivalent to the external signal, and clamps the intermediate signal to a second voltage lower than the first voltage when receiving the first control signal. The level keeper circuit pulls the intermediate signal up to a third voltage equal to or lower than the first voltage when receiving the second control signal. The buffer circuit receives the intermediate signal and outputs the internal signal.

[0021] In the high-voltage input tolerant receiver according to the invention, when the external signal is lower than the first voltage, i.e. equal to or lower than the high voltage limit of the internal elements, the control circuit does not output the first and second control signals. At this time,

the level keeper circuit is not active, and the first clamp circuit outputs the external signal input from the pad as the intermediate signal. Thus, when the external signal is equal to or lower than the first electric potential, even if the external signal is an analog signal, it is not distorted in the high-voltage input tolerant receiver.

[0022] However, when the external signal is higher than the first voltage, the intermediate signal is input to the buffer circuit after being clamped to the second voltage by the first clamp circuit and pulled up to the third voltage by the level keeper circuit. Thus, even an external signal in excess of the high voltage limit of the internal elements of the receiver is input to the high-voltage input tolerant receiver the internal elements are not damaged because the intermediate signal input into the buffer circuit is equal to or less than the high voltage limit of the internal elements. Further, since the first clamp circuit is enabled when the external signal becomes higher than the first voltage, the amount of current flowing through the level keeper circuit can be reduced, thereby reducing the power consumption of the high-voltage input tolerant receiver.

[0023] Preferably, the first clamp circuit includes a first n-channel transistor and a first p-channel transistor. The

first n-channel transistor having a gate to receive the third voltage, which corresponds to a defined input/output standard voltage. The first p-channel transistor, connected in parallel with the first n-channel transistor, has a gate to receive the first control signal.

[0024] When the external signal is equal to or lower than the first voltage and less than a threshold voltage of the first p-channel transistor, the first p-channel transistor is turned off. However, since the value that is the result of the subtraction of the source voltage (external signal) from the gate voltage of the first n-channel transistor is larger than a threshold voltage of the first n-channel transistor, the first n-channel transistor is fully turned on. Conversely, when the external signal exceeds the threshold voltage of the first p-channel transistor, since the value that is the result of the subtraction of the gate voltage from the source voltage (external signal) of the first p-channel transistor also exceeds the threshold, the first p-channel transistor is fully turned on.

[0025] It is apparent from the above-mentioned results that when the external signal is equal to or lower than the first voltage, either of the first n-channel transistor and the first p-channel transistor remains in the ON state, and

therefore the intermediate signal becomes equal to the external signal.

[0026] Further, when the external signal is higher than the first voltage, the first p-channel transistor receives the first control signal at its gate. As a result, the first p-channel transistor is turned off. Then, since the intermediate signal is clamped to the second voltage by the first n-channel transistor, the buffer circuit does not receive any signal higher than the first voltage, thereby preventing the internal elements of the high-voltage input tolerant receiver from being destroyed.

[0027] Preferably, the buffer circuit includes inverters to receive the intermediate signal, and the level keeper circuit includes a second p-channel transistor and a third p-channel transistor. The second p-channel transistor has a source to receive the third voltage and a gate to receive the second control signal. The third p-channel transistor, connected between the drain of the second p-channel transistor and the output node of the first clamp circuit, has a gate to receive an output signal from the inverters.

[0028] In this case, when the external signal voltage is higher than the first voltage, the second p-channel transistor is turned on in response to receiving the second control sig-

nal, and further the third p-channel is turned on. As a result, the level keeper circuit pulls the intermediate signal clamped to the second voltage up to the third voltage. Conversely, when the external signal is less than the fist voltage, the second p-channel transistor is turned off, and the level keeper circuit is not active. As a result, the amount of current in the level keeper circuit is reduced compared to prior art solutions, and enables a reduction in power consumption of the high-voltage input tolerant receiver as compared to prior art receiver circuits.

[0029] Preferably, the control circuit includes a switch, a second clamp, and a differential amplifier circuit. The switch outputs the first control signal equivalent to the external signal when the external signal is higher than the first voltage. The second clamp circuit holds the first control signal lower than the first voltage when receiving the first control signal. The differential amplifier circuit receives the clamped first control signal and outputs the second control signal.

[0030] In this case, the switch does not output the first control signal until the external signal becomes higher than the first voltage. Then, when the external signal becomes higher than the first voltage, the switch outputs the first

control signal equivalent to the external signal to the first clamp circuit so that the first clamp circuit can hold the external signal at the second voltage as soon as the external signal becomes higher than the first voltage.

[0031] The second clamp circuit receives and clamps the first control signal to the second voltage, and outputs the clamped signal to the differential amplifier circuit. The differential amplifier circuit does not receive any signal higher than the first voltage, thereby preventing the internal elements from being destroyed.

[0032] The differential amplifier circuit receives the first control signal clamped by the second clamp circuit, and outputs the second control signal. It allows the level keeper circuit to operate only when the voltage of the external signal is higher than the first voltage, and hence it can reduce the amount of current flowing in the level keeper circuit.

Brief Description of Drawings

[0033] Fig. 1 illustrates a circuit diagram showing the general structure of a high-voltage input tolerant receiver according to an embodiment of the invention.

[0034] Fig. 2 illustrates a timing chart corresponding to the operation of the high-voltage input tolerant receiver shown in Fig. 1.

[0035] Fig. 3 illustrates a circuit diagram showing the general structure of a conventional high-voltage input tolerant receiver.

[0036] Fig. 4 illustrates a timing chart showing the operation of the high-voltage input tolerant receiver shown in Fig. 3.

[0037] Fig. 5 illustrates a circuit diagram showing the general structure of a reset circuit.

Detailed Description

[0038] Referring to the accompanying drawings, an embodiment of the invention will now be described in detail. In the drawings, identical or equivalent portions are given the same reference numerals to invoke the same descriptions.

[0039] Structure of High-Voltage Input Tolerant ReceiverReferring to Fig. 1, a high-voltage input tolerant receiver 1 includes a pad 2, a clamp circuit 3, a level keeper 6, a control circuit 4, an operating circuit 7, a hysteresis circuit 5, a buffer circuit 15, and an output node 8.

[0040] The clamp circuit 3 is connected between the pad 2 and the input node of the buffer circuit 15. The clamp circuit 3 includes an n-channel MOS transistor N1 and a p-channel MOS transistor P1. The n-channel MOS transistor N1 and the p-channel MOS transistor P1 are connected in parallel. The gate of the n-channel MOS transistor N1 is connected

to a 3.3V power-supply potential node 10. The gate of the p-channel MOS transistor P1 is connected to the control circuit 4. The clamp circuit 3 receives an external signal ϕC input from PAD 2 and outputs an intermediate signal ϕD.

[0041] The control circuit 4 includes a switch circuit 14, a clamp circuit 12, and a differential amplifier circuit 9. The switch circuit 14 includes a p-channel MOS transistor P10. The p-channel MOS transistor P10, connected between the pad 2 and the operating circuit 7, receives a voltage Vg at its gate. The switch circuit 14 receives the external signal ϕC and outputs a control signal ϕE. When the external signal ϕC exceeds 3.6V, the p-channel MOS transistor P10 is turned on to make the control signal ϕE equivalent to the external signal ϕC. The voltage Vg is so set that the p-channel MOS transistor P10 is turned on when the external signal ϕC exceeds 3.6V. If the threshold voltage of the p-channel MOS transistor P10 is 1.64V, the voltage Vg will be set to 1.96V. The control signal ϕE is output to the clamp circuit 12 and the gate of the p-channel MOS transistor P1 in the clamp circuit 3.

[0042] The clamp circuit 12 includes an n-channel MOS transistor N8. The n-channel MOS transistor N8, connected between

the switch circuit 14 and the gate of a p-channel MOS transistor P13, receives a signal from the 3.3V power-supply potential node 10. The clamp circuit 12 receives the control signal ϕE and outputs a signal ϕG. When the control signal ϕE is larger than $3.3V-V_{thN8}$, the clamp circuit 12 clamps the signal ϕG to $3.3V-V_{thN8}$ where $3.3V-V_{thN8}$ is a threshold voltage of the n-channel MOS transistor N8.

[0043] The differential amplifier circuit 9 includes p-channel MOS transistors P11 to P14, n-channel MOS transistors N9 and N10, and a resistor element R1. The p-channel MOS transistors P11, P12, and the resistor element R1 form a constant current generator. The p-channel MOS transistors P11 and P12 form a current mirror. The sources of the p-channel MOS transistors P11 and P12 are both connected to the 3.3V power-supply potential node 10. The resistor R1 is connected between the drain of the p-channel MOS transistor P11 and a ground potential node 30. The sources of the p-channel MOS transistors P13 and P14 are both connected to the drain of the p-channel MOS transistor P12. The n-channel MOS transistor N9 is connected between the p-channel MOS transistor P13 and the ground potential node 30, while the n-channel MOS transistor N10 is connected between the p-channel MOS tran-

sistor P14 and the ground potential node 30. The n-channel MOS transistors N9 and N10 form a current mirror. The gate of the p-channel MOS transistor P14 receives a reference potential Vref (=1.65V), while the gate of the p-channel MOS transistor P13 receives the output signal ϕG from the clamp circuit 12. The differential amplification circuit 9 outputs a control signal ϕF from its output node 11.

[0044] The buffer circuit 15 includes inverters IV1 to IV4. The inverters IV1 to IV4 are connected in series between the clamp circuit 3 and the output node 8. The inverter IV1 includes a p-channel MOS transistor P2 and an n-channel MOS transistor N2, which are connected in series between the 3.3V power-supply potential node 10 and the ground potential node 30. The inverter IV2 includes a p-channel MOS transistor P3 and an n-channel MOS transistor N3, which are connected in series between the 3.3V power-supply potential node 10 and the ground potential node 30. The inverter IV3 includes a p-channel MOS transistor P4 and an n-channel MOS transistor N4, which are connected in series between an internal power-supply potential Vdd node 20 and the ground potential node 30. The inverter IV4 includes a p-channel MOS transistor P5 and

an n-channel MOS transistor N5, which are connected in series between the internal power-supply potential Vdd node 20 and the ground potential node 30. The inverter IV4 outputs an internal signal ϕB to the output node 8.

[0045] The level keeper 6 includes p-channel MOS transistors P8 and P9 connected in series. The source of the p-channel MOS transistor P8 is connected to the 3.3V power-supply potential node 10, and the gate thereof receives the control signal ϕF output from the control circuit 4. The drain of the p-channel MOS transistor P9 is connected with the output node of the clamp circuit 3 and the input node of the inverter IV1, and the gate thereof receives an output signal from the inverter IV1.

[0046] The hysteresis circuit 5 is a circuit provided to reduce noise. The hysteresis circuit 5 includes inverters IV5 and IV6 connected in series. The operating circuit 7, also shown in Fig. 1 is a circuit for actuating the high-voltage input tolerant receiver 1. The operating circuit 7 includes n-channel MOS transistors N11 and N12 to whose gates a receiver enable signal RE for activating the high-voltage input tolerant receiver 1 is input.

[0047] Operation of the High-Voltage Input Tolerant ReceiverReferring next to Fig. 2, the operation of the high-voltage

input tolerant receiver 1 is described when the external signal ϕC is periodically varied from 0 to 5.5V. Note that during operation the receiver enable signal RE input to the operating circuit 7 is a logic high, which enables the high-voltage input tolerant receiver 1.

[0048] At time t1, the external signal ϕC input from the pad 2 is 0V.

[0049] The clamp circuit 3 outputs the intermediate signal ϕD of 0V that is equivalent to the external signal ϕC. Specifically, in the clamp circuit 3, the result of the subtraction of the source voltage (= external signal ϕC) from the gate voltage (3.3V) of the n-channel transistor N1 is larger than a threshold voltage V_{thN1} of the n-channel transistor N1. Therefore, the n-channel transistor N1 is fully turned on, and the output signal (= intermediate signal ϕD) becomes 0V which is identical to the voltage of the external signal ϕC at time t0.

[0050] The switch circuit 14 outputs the control signal ϕE which is equal to 0V at time t0. In the switch circuit 14, the result of the subtraction of the gate voltage Vg (= 1.96V) from the source voltage (ϕC = 0V) of the p-channel MOS transistor P10 becomes smaller than a threshold voltage V_{thp10} (= 1.64V) of the p-channel MOS transistor P10. Thus,

since the p-channel MOS transistor P10 is in the OFF state and the n-channel MOS transistors N11 and N12 are in the ON state, the control signal ϕE output from the p-channel MOS transistor P10 is 0V.

[0051] The gate of the n-channel MOS transistor N8 in the control circuit 4 is tied to 3.3V and receives the 0V control signal ϕE at its source. As a result, since the gate-source voltage exceeds the threshold voltage V_{thN8} of the n-channel MOS transistor N8, the n-channel MOS transistor N8 is fully turned on, and the signal ϕG output from the n-channel MOS transistor N8 becomes 0V, which is identical to the voltage of the control signal ϕE a time t0.

[0052] In the differential amplifier circuit 9, the gate of p-channel MOS transistor P13 receives the signal ϕG of 0V. Since the voltage of the signal ϕG is smaller than the reference voltage Vref (= 1.65V), the control signal ϕF output from the output node 11 becomes high (= 3.3V). Upon receipt of the logic high control signal ϕF, since the p-channel MOS transistor P8 is turned off, the level keeper 6 is not active.

[0053] During the period from time t1 to time t2 when the external signal ϕC becomes 3.6V, the external signal ϕC increases its voltage at a constant rate per unit time. During

this period, since the external signal ϕC remains less than 3.6V, the result of the subtraction of the gate voltage Vg (= 1.96V) from the source voltage (external signal ϕC) of the p-channel MOS transistor P10 does not exceed the threshold voltage V_{thp10} (= 1.64V). Therefore, the p-channel MOS transistor P10 remains in the OFF state, and the control signal ϕE remains at 0V. Upon receipt of the signal ϕE of 0V, the clamp circuit 12 outputs the signal ϕG of 0V. Since the differential amplifier circuit 9 receives the signal ϕG of 0V, it outputs the logic high control signal ϕF. Then, since the level keeper 6 receives the logic high control signal ϕF, it remains inactive.

[0054] During the period from time t1 to time t2, the intermediate signal ϕD output form the clamp circuit 3 becomes equivalent to the external signal ϕC. Specifically, when the external signal ϕC is less than the threshold voltage V_{thP1} of the p-channel MOS transistor P1, the p-channel MOS transistor P1 is turned off, but since the gate-source voltage (= 3.3V - external signal ϕC) of the n-channel MOS transistor N1 is larger than the threshold voltage V_{thN1}, the n-channel MOS transistor N1 is fully turned on.

[0055] However, when the external signal ϕC exceeds the threshold voltage V_{thP1}, since the result of the subtraction

of the gate voltage (= control signal ϕE = 0V) from the source voltage (= external signal ϕC) of the p-channel MOS transistor P1 exceeds the threshold V_{thP1}, the p-channel MOS transistor P1 is fully turned on.

[0056] From the above results, it is found that either the n-channel MOS transistor N1 or the p-channel MOS transistor P1 remain in the ON state in the clamp circuit 3 during the period from time t1 to time t2. Therefore, since the intermediate signal ϕD becomes equivalent to the external signal ϕC, the external signal ϕC is not distorted in the high-voltage input tolerant receiver 1 even though it is an analog signal.

[0057] After time t2, the external signal ϕC exceeds 3.6V. At this time, since the result of the subtraction of the gate voltage Vg (= 1.96V) from the source voltage (= external signal ϕC) in the p-channel MOS transistor P10 exceeds the threshold voltage V_{thP10} (= 1.64V), the p-channel MOS transistor P10 is fully turned on to make the control signal ϕE equivalent to the external signal ϕC.

[0058] In the clamp circuit 3, the p-channel MOS transistor P1 receives the external signal ϕC at its source and the control signal ϕE equivalent to the external signal ϕC at its gate. Therefore, the p-channel MOS transistor P1 is

turned off. On the other hand, since the n-channel MOS transistor N1 receives the external signal ϕC at its drain and 3.3V at its gate, it outputs a signal clamped to 3.3V-V_{thN1}. As a result, the intermediate signal ϕD output from the clamp circuit 3 is clamped to 3.3 V-V_{thN1}. However, as will be described later, since the intermediate signal ϕD is pulled up to 3.3V by the level keeper 6, the intermediate signal ϕD clamped to 3.3 V-V_{thN1} does not appear in Fig. 2 until immediately after time t2.

[0059] In the control circuit 4, since the gate of n-channel MOS transistor N8 is tied to 3.3V and the drain is coupled to control signal ϕE, the signal ϕG is clamped to 3.3 V-V_{thN8}. Since the clamp circuit 12 clamps the signal ϕG, it does not output the signal ϕG at a level higher than the upper voltage limit to the p-channel MOS transistor P13 of the differential amplifier circuit 9. Therefore, the reliability of the gate oxide film of the p-channel MOS transistor P13 can be secured, protecting the differential amplifier circuit 9 from being damaged or destroyed. Upon receipt of the signal ϕG of 3.3V-V_{thN8}, the differential amplifier circuit 9 outputs a logic low (0v) control signal ϕF from output node 11.

[0060] In the level keeper 6, since the gate of p-channel MOS

transistor P8 receives the control signal ϕF of 0V and the source is tied to 3.3V, the result of the subtraction of the gate voltage from the source voltage exceeds the threshold voltage V_{thP8}. Therefore, the p-channel MOS transistor P8 is fully turned on. On the other hand, the gate of p-channel MOS transistor P9 receives the output signal from the inverter IV1. The output signal of the inverter IV1 has been 0V since the external signal ϕC exceeded the threshold voltage V_{thN2} of the n-channel MOS transistor N2 after time t1. Therefore, the gate of p-channel MOS transistor P9 receives the output signal of 0V at time t2, and is turned on. Thus, since the p-channel MOS transistors P8 and P9 are both turned on, the level keeper 6 pulls the intermediate signal ϕD up to 3.3V.

[0061] According to the above-described operation, after the external signal ϕC exceeds 3.6V, the intermediate signal ϕD is fixed at 3.3V. At this time, although current I1 flows from the node 13 to the level keeper 6, the amount of current I1 can be significantly less than in the conventional level keeper 60. This is because the level keeper 6 is active only when the external signal ϕC exceeds 3.6V, rather than when the output signal of the inverter IV1 is a logic low.

[0062] After time t3, the external signal ϕC decreases from 5.5V at a constant rate per unit time. After time t4, the external signal ϕC becomes equal to or less than 3.6V and the result of the subtraction of the gate voltage Vg from the source voltage (external signal ϕC) of the p-channel MOS transistor P10 becomes smaller than the threshold V_{thP10}. Therefore, the p-channel MOS transistor P10 is turned off to cause a rapid voltage drop of the control signal ϕE. Then, when the result of the subtraction of the gate voltage (control signal ϕE) from the source voltage (external signal ϕC) of the p-channel MOS transistor P1 exceeds the threshold voltage V_{thP1}, the p-channel MOS transistor P1 is turned on again. As a result, the intermediate signal ϕD output from the clamp circuit 3 becomes equivalent to the external signal ϕC again.

[0063] Since the gate-source voltage of the n-channel MOS transistor N8 in the control circuit 4 becomes larger than the threshold V_{thN8}, the output signal ϕG is equivalent to the control signal ϕE. At time t5, signal ϕG becomes lower than the reference voltage Vref (= 1.65V) and the differential amplifier circuit 9 outputs the control signal ϕF of 3.3V. At this time, since the result of the subtraction of the gate voltage (3.3V) from the source voltage (3.3V) of

the p-channel MOS transistor P8 in the level keeper 6 becomes zero, that is, smaller than the threshold voltage V_{thP8}, the p-channel MOS transistor P8 is turned off. In other words, since the level keeper 6 stops pulling up the intermediate signal ϕD, the intermediate signal ϕD becomes equivalent to the external signal ϕC. Although current I1 flows from the level keeper 6 to the node 13 until the level keeper 6 is disabled, the amount of current is substantially lower than in prior art receiver circuits because the operation of the level keeper 6 is stopped at time t5.

[0064] In the embodiment, based on the assumption that the voltage limit of the internal elements of the high-voltage input tolerant receiver 1 is 3.6V, the gate voltage Vg is set to 1.96V so that the p-channel MOS transistor P10 in the control circuit 4 will be fully turned on when the external signal ϕC exceeds 3.6V. This is to prevent the internal elements from being destroyed from a high voltage external signal ϕC larger than the limit of the internal elements of the high-voltage input tolerant receiver 1. Therefore, even if the withstand voltage of the internal elements is any value, other than 3.6V, the gate voltage Vg of the p-channel MOS transistor P10 may be determined based on

the voltage limit of the internal elements of the high-voltage input tolerant receiver 1. Another value may be substituted for the 3.3V power-supply provided it is lower than the voltage limit of the internal elements.

[0065] While the invention has been described in detail, the foregoing description is in all aspects illustrative and not restrictive. It is understood that numerous other modifications and variations can be devised without departing from the scope of the invention.